University of Dayton

ECE

Mumma Radar Lab

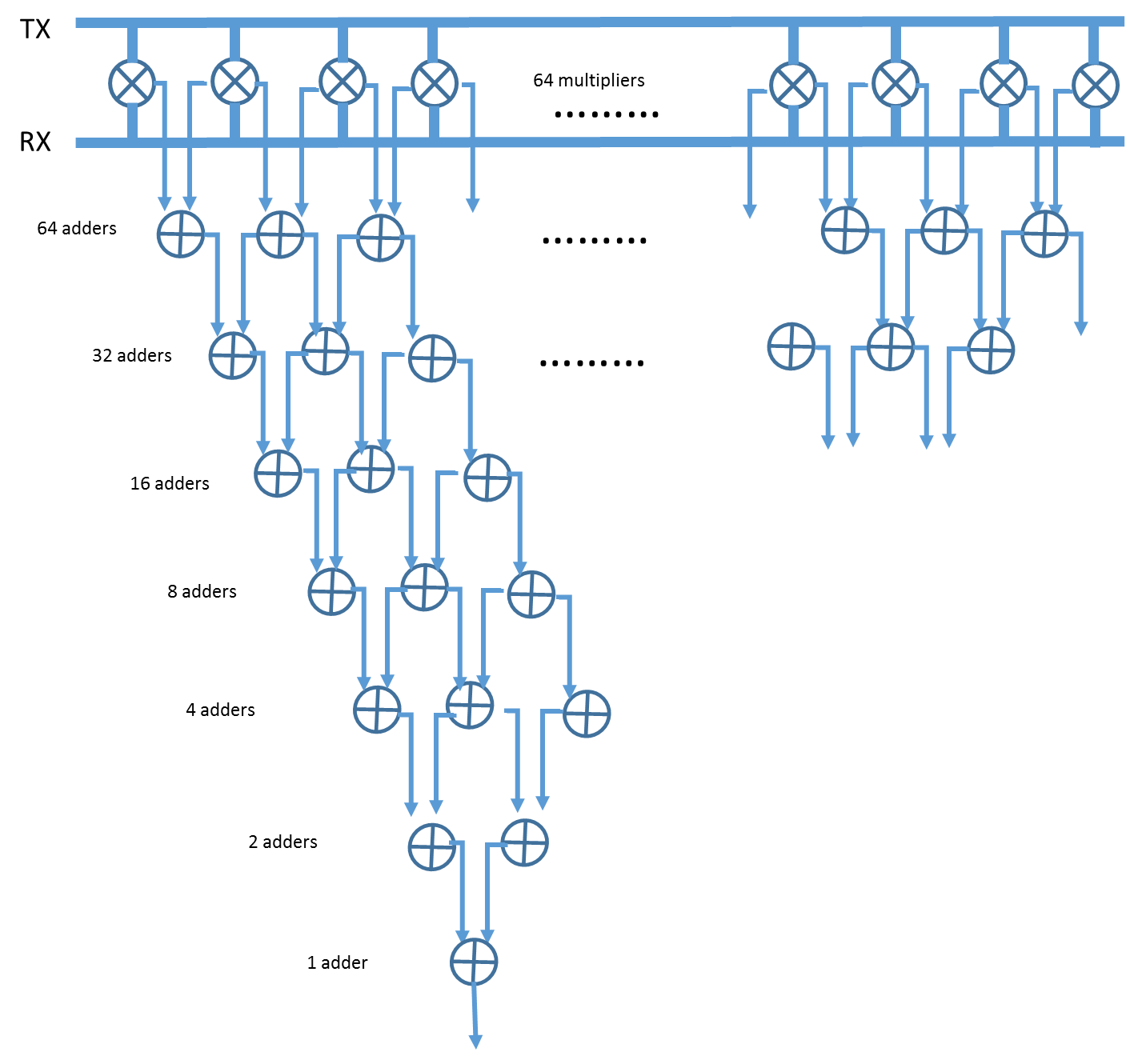
Comprehensive VHDL

Fall 2016

Homework 6

Convolution using VHDL

Design VHDL block to convolve two signals (TX, RX), see the block bellow.

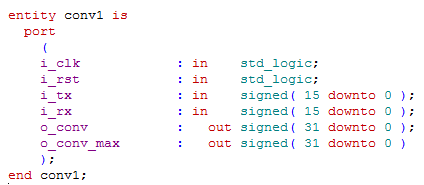


You have given two text files (tx.txt and rx.txt).

Recommended steps:

* Read both files (transmitted, and received signals), both 64 integers
* Save the TX signal in a ram.
* Flip the TX signal when you read it out of the ram.
* Create adder and multiplier blocks in VHDL. Then instantiate them on your main code.
* Use *Generate Statement to* instantiate64 multipliers to multiply TX by RX.
* Use *Generate Statement to* instantiateadders to add the result of the multiplication above (no saturation).
* You can use the layout on the diagram above (64 adders, 32 adders….…2 adders, then one adder).
* The final addition is your convolution result.
* Record the peak value of your convolution.

Please use the following entity:

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**Plot the result of your convolution signal in MATLAB.**